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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/805,182	03/19/2004	Rino Micheloni	NUM.0098US	7411
76446	7590	12/01/2009		
Trop, Pruner & Hu, P.C. 1616 S. Voss Road, Suite 750 Houston, TX 77057-2631			EXAMINER	
			MANOSKEY, JOSEPH D	
		ART UNIT	PAPER NUMBER	
		2113		
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		12/01/2009	PAPER	

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/805,182	Applicant(s) MICHELONI ET AL.
	Examiner JOSEPH D. MANOSKEY	Art Unit 2113

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
 - If no period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
 - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED. (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 19 August 2009.
 2a) This action is FINAL. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-21 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) 1-18 is/are allowed.
 6) Claim(s) 19-21 is/are rejected.
 7) Claim(s) _____ is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on 19 March 2004 is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) Notice of References Cited (PTO-892)
 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
 3) Information Disclosure Statement(s) (PTO/GS-68)
 Paper No(s)/Mail Date _____
- 4) Interview Summary (PTO-413)
 Paper No(s)/Mail Date _____
 5) Notice of Informal Patent Application
 6) Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 19-21 are rejected under 35 U.S.C. 102(e) as being anticipated by Longwell, et al. U.S. Patent 7,134,069, hereinafter referred to as "Longwell".
3. Referring to claim 19 and 20, Longwell teaches a memory system with integrated circuits such as DRAM (See Fig. 1, Col. 1, lines 5-8 and Col. 3, lines 38-40). Longwell teaches error detection and correction (EDAC) units that includes both word-wise error detection and correction (WEDAC) units and bit-wise error detection and correction (BEDAC) units (See Col. 3, lines 15-37). The BEDAC unit is capable of correcting double-bit errors which the WEDAC is not capable of doing (See Col. 3, lines 15-37). This is interpreted as a method, comprising: storing, in a non-volatile solid-state memory location of a device, data having associated therewith at least one storage error of a plurality of storage-error types; and correcting, at the memory location, a first-type error

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of the plurality of storage-error types. This is also interpreted as further comprising generating, at the memory location, an interrupt-request signal indicating detection of a second-type error of the plurality of storage-error types.

4. Referring to claim 21, Longwell teaches a memory system with integrated circuits such as DRAM (See Fig. 1, Col. 1, lines 5-8 and Col. 3, lines 38-40). Longwell teaches error detection and correction (EDAC) units that includes both word-wise error detection and correction (WEDAC) units and bit-wise error detection and correction (BEDAC) units (See Col. 3, lines 15-37). The BEDAC unit is capable of correcting double-bit errors which the WEDAC is not capable of doing (See Col. 3, lines 15-37). This is interpreted as an electronic system, comprising: a first integrated circuit having a non-volatile solid-state memory to store data having associated therewith at least one storage error of a plurality of storage-error types, the memory to correct a first-type error of the plurality of storage-error types; and a second integrated circuit coupled to the first circuit, the second integrated circuit having processor to correct a second-type error of the plurality of storage-error types.

Allowable Subject Matter

5. Claims 1-18 are allowed.

Response to Arguments

6. Applicant's arguments, see page 6 of amendment, filed 19 August 2009, with respect to claims 1-3 and 9-18 have been fully considered and are persuasive. The 35 U.S.C. 102(e) rejection of the claims has been withdrawn.

7. Regarding claims 19-21, the Applicant did not amend or argue the rejections of claims 19-21 therefore the rejections still stand.

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JOSEPH D. MANOSKEY whose telephone number is (571)272-3648. The examiner can normally be reached on Mon.-Fri. (7:30am to 4pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JDM
November 24, 2009

/Robert W. Beausoliel, Jr./
Supervisory Patent Examiner, Art Unit 2113